Product Features

Frequency: 100MHz ~ 4GHz

Attenuation Range: 0.5dB LSB steps to 31.5dB

Both Serial and Parallel Control

CMOS-/TTL-Compatible Control

Single Supply Voltage: 5V

Package: QFN24

Application

Communication Base Stations

Test Equipment

Point-to-Point Communication

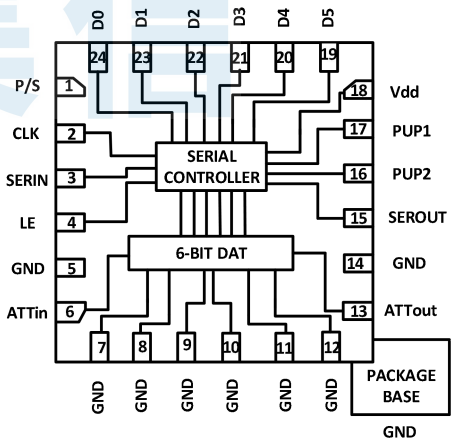
Radio

Navigation Equipment

General Description

BR9155S is a wideband MMIC 6-bit serial/parallel digital attenuator designed using GaAs process with a 31.5 dB attenuation control range in 0.5 dB steps over the frequency range from 100MHz to 4GHz. The digital attenuator provides typical insertion loss less than 3dB, and excellent attenuation accuracy and high input linearity. The product operates with a single +5V positive supply voltage, and provides a CMOS-/TTL-compatible control interface. The device also features a user-selectable power-up state and a serial output port for cascading other serial controlled components.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BR9155S	QFN24	100MHz~4GHz 6-bit Serial/Parallel Digital Attenuator

Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Insertion Loss	0.1GHz to 1.5GHz	-1.5	-1.6	-1.7	dB
	1.5GHz to 3.0GHz	-1.7	-2.1	-2.7	
	3.0GHz to 4.0GHz	-2.7	-3.0	-3.5	
Attenuation Range	0.1GHz to 4.0GHz	0.5	-	31.5	dB
Input Return Loss	0.1GHz to 4.0GHz	-	-17	-	dB
Output Return Loss	0.1GHz to 4.0GHz	-	-18	-	dB
Attenuation Accuracy: (Reference state Insertion Loss) 0.5dB ~ 16dB attenuation state 16.5dB ~ 31.5dB attenuation state	0.1GHz to 4.0GHz	+ / - 0.4 + / - 1.4			dB dB
Input Power for 1dB Compression	0.6GHz to 2.7GHz	30.6	31.3	32.3	dBm
Input Third-Order Interception	0.1GHz to 2.8GHz	45.8	-	-	dBm
Switching Characteristics T_{rise} (50% CTL to 90% RF) T_{fall} (50% CTL to 10% RF)	Test at a frequency of 200MHz and an attenuation of 31.5dB	- -	94 40	- -	ns ns
Test Condition: Vdd=+5V, I=4mA, IIP3 spacing=1MHz, Pin=15dBm/tone, Temp=+25℃					

Absolute Maximum Ratings

Maximum Supply Voltage (Vdd) : +7V;

Maximum RF input Power:+25dBm;

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

Recommended Operating Conditions

Supply Voltage: +5V;

Supply Current: 4mA;

Control Voltage: 0 ~ 0.8V (Low Level);

2.7V ~ Vdd (High Level);

PUP1/PUP2 Control Voltage:

0 ~ 0.8V (Low Level);

Vdd-0.5 ~ Vdd (High Level);

Storage Temperature: -65℃ ~ +150℃;

Operating Temperature: -55℃ ~ +125℃;

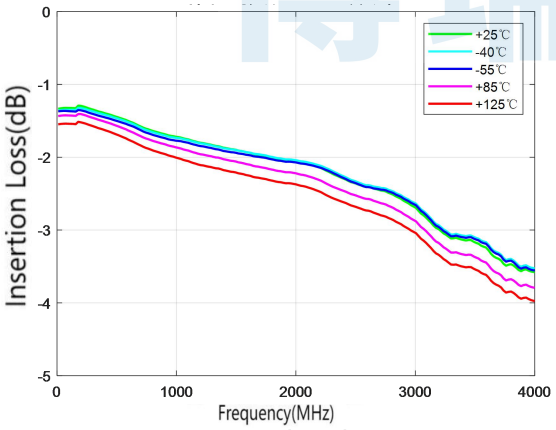
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

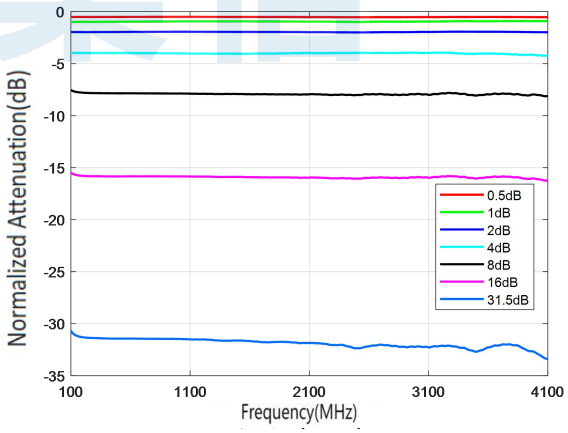
OBSERVE HANDLING PRECAUTIONS

Typical Performance (EVB test results)

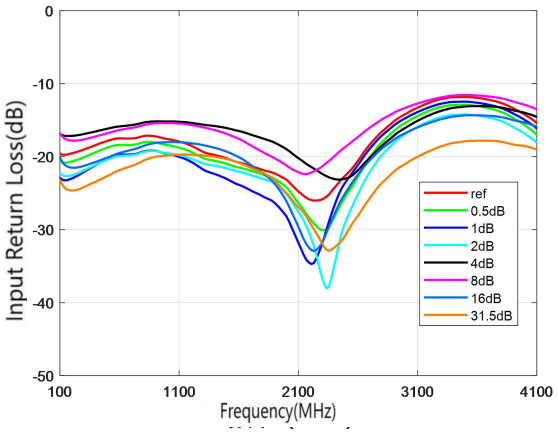
Parameters	Typ.						Units
Frequency	100	500	1000	2000	3000	4000	MHz
Reference State Insertion Loss	-1.37	-1.48	-1.58	-1.87	-2.63	-3.37	dB
Attenuation Accuracy (0.5dB)	0.01	0.03	0.04	0.02	0.03	0.03	dB
Attenuation Accuracy (1 dB)	0.04	0.08	0.10	0.09	0.08	0.15	dB
Attenuation Accuracy (2 dB)	0.08	0.10	0.10	0.08	0.10	0.09	dB
Attenuation Accuracy (4 dB)	0.09	0.07	0.03	0.05	0.15	-0.13	dB
Attenuation Accuracy (8 dB)	0.45	0.21	0.15	0.14	0.06	0.02	dB
Attenuation Accuracy (16 dB)	0.51	0.25	0.21	0.15	0.11	-0.07	dB
Attenuation Accuracy (31.5dB)	0.75	0.20	0.09	-0.22	-0.57	-1.62	dB
Input Return loss	-16.6	-17.2	-17.4	-22.5	-14.3	-13.6	dB
Output Return loss	-16.4	-17.9	-18.5	-24.9	-14.7	-14.0	dB
Input Power for 1dB Compression	-	30.64	31.32	32.16	-	-	dBm
Switching Characteristics	94 (T_{rise})			42 (T_{fall})			ns
Test Conditions: Vdd=+5V, I=4mA, Temp=+25℃							



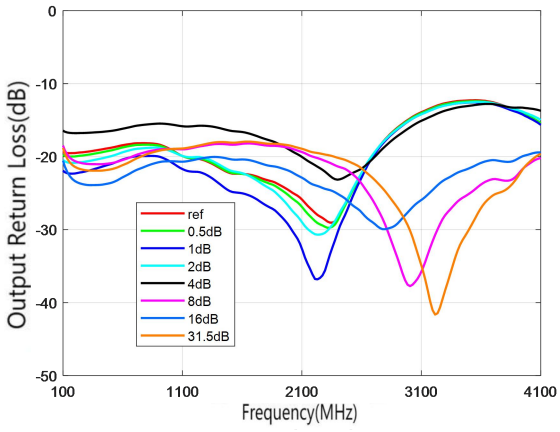
Insertion Loss



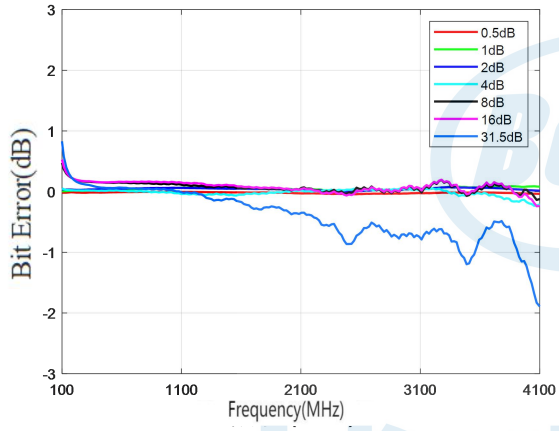
Nornmalized Attenuation



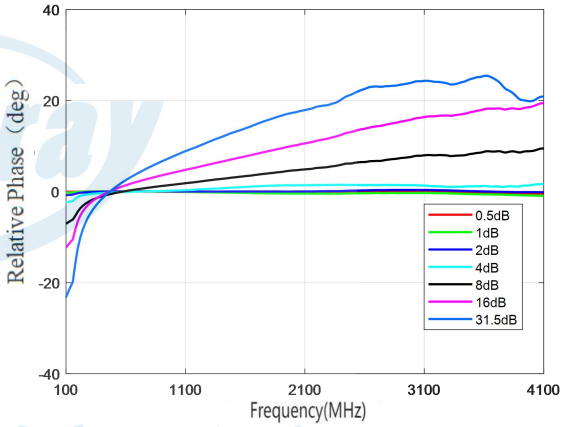
Input Return Loss



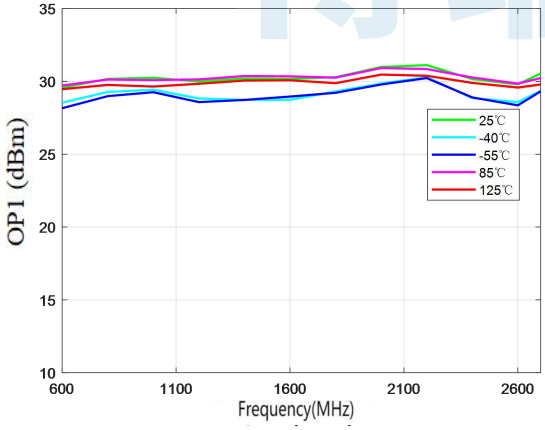
Output Return Loss



Bit Error

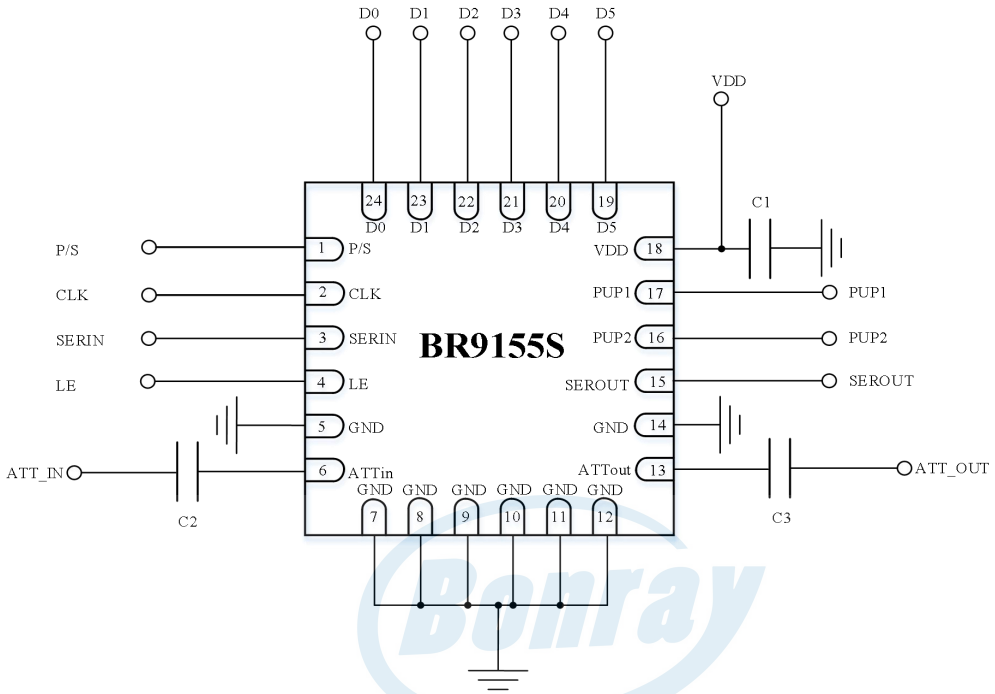


Relative Phase



Output Power for 1dB Compression

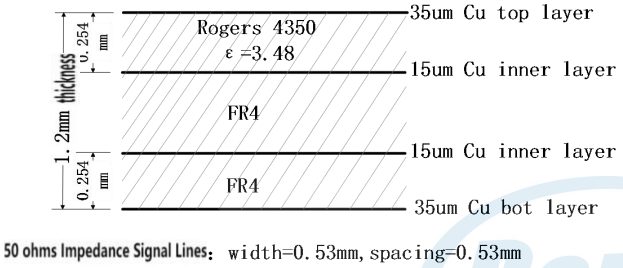
Typical Application Schematic



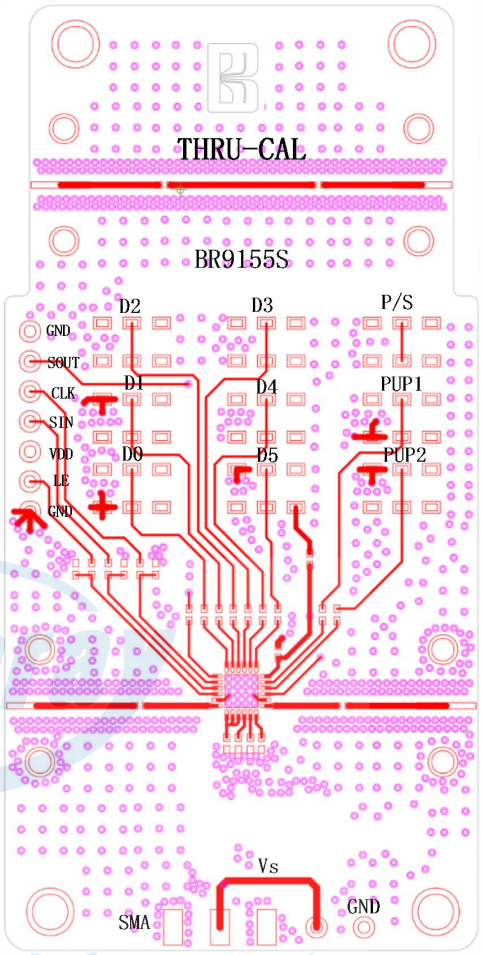
Bill of Material

Designator	Package	Description	Part Number
C1	0402	1000pF	GRM1555C1H102JA01D
C2, C3	0402	100pF	GRM1555C1H101JA01D

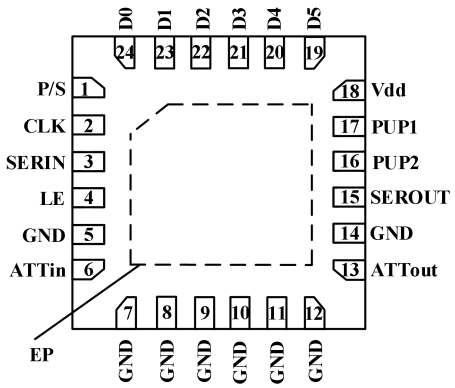
PCB Evaluation Board



50 ohms Impedance Signal Lines: width=0.53mm, spacing=0.53mm



Pin Configuration and Description



Pin Number	Pin Name	Description
1	P/S	Parallel/Serial mode selection pin. See Mode Selection Truth Table.
5, 7 to 12,14	GND	RF/DC ground pins. Connect to ground.
6, 13	ATTin, ATTout	Attenuator RF input/output pins. DC block is required.
15	SEROUT	Serial interface data output pin. Serial input data is delayed by six clock cycles.
19 to 24	D5-D0	Parallel control voltage input pins. Select the required attenuation. See Parallel Control Voltage Truth Table.
2	CLK	Serial interface clock input pin.
3	SERIN	Serial interface data input pin.
4	LE	Latch enable input pin. See Mode Selection Truth Table.
16 or 17	PUP2,PUP1	Power-up state selection pins. See PUPx Truth Table.
18	Vdd	Power supply pin.
-	EP	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistant; see PCB Mounting Pattern for suggested footprint.

Mode Selection

There are three control modes for BR9155S: Power-up control mode, Serial control mode, and Parallel control mode.

Mode Selection Truth Table

LE	P/S	Control Mode
Low	X	Power-up
High	Low	Parallel
High	High	Serial

Power-up Interface

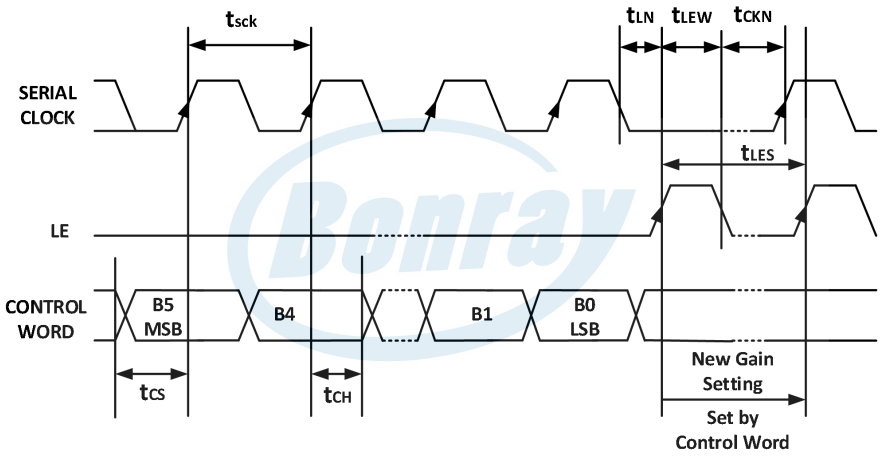
The BR9155S uses the PUP1 and PUP2 control voltage inputs to set the attenuation value to a known value at power-up before the initial control data word is provided in either serial or parallel mode. When the attenuator powers up with LE set to low, the state of PUP1 and PUP2 determines the power-up state of the device per the PUPx Truth Table.

PUPx Truth Table

LE	PUP1	PUP2	Attenuation State
Low	Low	Low	31.5dB
Low	High	Low	-24dB
Low	Low	High	-16dB
Low	High	High	Insertion loss (Reference State)
High	X	X	Determined by D0 to D5

Serial Mode Interface

The BR9155S has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to high. In serial mode, the 6-bit SERIN data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept high.



Timing Specificationse Table

Numbers	Parameters	Typ.	Number	Parameters	Typ.
1	Minimum serial period (tSCK)	100ns	5	Minimum LE pulse width (tLEW)	10ns
2	Control setup time (tCS)	20ns	6	Minimum LE pulse spacing (tLES)	630ns
3	Control hold time (tCH)	20ns	7	Serial clock hold time from LE (tCKN)	10ns
4	LE setup time (tLN)	10ns			

Parallel Mode Interface

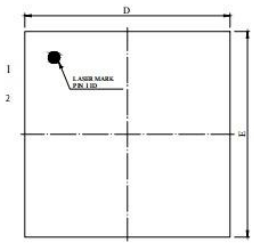
The BR9155S has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode. The parallel control interface is activated when P/S is set to low and LE set to high.

Parallel Control Voltage Truth Table

Digital Control Input						Attenuation State RF1/RF2
D5 16dB	D4 8dB	D3 4dB	D2 2dB	D1 1dB	D0 0.5dB	
High	High	High	High	High	High	Insertion Loss(Reference)
High	High	High	High	High	Low	0.5 dB
High	High	High	High	Low	High	1 dB
High	High	High	Low	High	High	2 dB
High	High	Low	High	High	High	4 dB
High	Low	High	High	High	High	8 dB
Low	High	High	High	High	High	16 dB
Low	Low	Low	Low	Low	Low	31.5dB

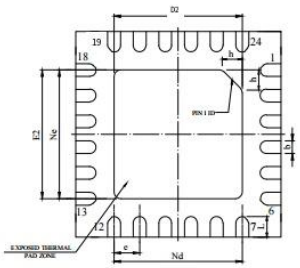
Note: Any combination of the control voltage input states shown in this table provides an attenuation approximately equal to the sum of the bits selected.

Package Dimensions (mm)

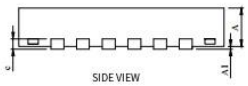


TOP VIEW

SIDE VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	0.01	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.35	0.40	0.45